What is Claimed is:

[c1] An on-chip logic analysis (OCLA) system comprising:

a single chip device internally including a signal processing unit, a plurality of memory blocks and a data capturing unit; and

a host unit externally provided to said single chip device and generating control signals to control said data capturing unit,

wherein said data capturing unit captures data processed by said signal processing unit in response to said control signals from said host unit and transfers said captured data to said host unit without interrupting operations of said signal processing unit.

[c2] The OCLA system of claim 1, further comprising:

a first signal path transferring a clock signal from said host unit to said data capturing unit; and

a second signal path transferring said control signals from said host unit to said data capturing unit and transferring said captured data from said data capturing unit to said host unit.

[c3] The OCLA system of claim 2, wherein said single chip device comprises:

a first pin utilized for providing said first signal path between said host unit and said data capturing unit; and

a second pin utilized for providing said second signal path between said host unit and said data capturing unit

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[c4] The OCLA system of claim 1, wherein said data capturing unit comprises:

a control unit controlling operations of said data capturing unit in response to the control signals from said host unit;

a buffer unit storing said data processed by said signal processing unit; and

a communication unit transferring said control signals from said host unit to said control unit and transferring said data captured by said buffer unit to said host unit.

[c5] The OCLA system of claim 4, wherein said buffer unit comprises a static random

access memory (SRAM).

[c6] The OCLA system of claim 4, wherein said control unit includes a trigger unit for monitoring said data processed by said signal processing unit to determine a current trigger mode of said OCLA system.

[c7] The OCLA system of claim 1, further comprising a user interface enabling a user to control said OCLA system and presenting said captured data to the user.

[c8] The OCLA system of claim 7, wherein said user interface is a graphic user interface (GUI).

[c9] The OCLA system of claim 7, wherein the host unit comprising:

an interface unit transferring said controls signals from said host system to said data capturing unit and transferring said captured data from said data capturing unit to said host unit; and

a memory unit storing said control signals and said captured data.

[c10] The OCLA system of claim 9, wherein said interface unit and said memory unit are implemented in a personal computer international standard architecture (PC ISA) interface card.

[c11] The OCLA system of claim 10, wherein said interface unit is implemented as a field programmable gate array (FPGA) attached on said PC ISA card.

[c12] The OCLA system of claim 7, wherein said user interface is synchronized with said host unit in a real-time basis.

[c13] The OCLA system of claim 1, wherein said data capturing unit determines which one of said plurality of memory blocks is active based on an internal chip enable signal of said single chip device.

[c14] The OCLA system of claim 1, wherein each unit of said control signals comprises:

a data portion designating at least one mask value, a match value and a trigger mode; and

a command portion designating a current operational mode to be

performed in response to a current unit of said control signal.

[c15] The OCLA system of claim 14, wherein said control unit loads a trace word from said captured data and performs multiplexing operations by using said mask value and match value.

[c16] The OCLA system of claim 15, wherein said multiplexing operations comprising:

a masking operation by bitwise ANDing said trace word and said mask value; and

a matching operation by bitwise eXclusive-ORing of said masked trace word and said match value.

[c17] An on-chip very high speed integrated circuit (VHSIC) hardware description language (VHDL) macro embedded in a single chip device comprising:

digital signal processing (DSP) core logic; and

on-chip logic analysis (OCLA) logic capturing data processed by said DSP core logic without interrupting operations of said DSP logic, wherein said OCLA logic is controlled by a host unit externally provided to said single chip device.

[c18] The VHDL macro of claim 17, wherein said OCLA logic comprises:

control logic for controlling operations of said OCLA logic in response to control signals from said host unit;

a buffer capturing data processed by said DSP core logic; and

communication logic for transferring said control signals and said captured data between said VHDL macro and said host unit.

[c19] A single chip device comprising:

a signal processing unit;

a plurality of memory blocks;

a on-chip logic analysis (OCLA) unit capturing data processed by said signal processing unit without interrupting operations of said signal processing unit, wherein said OCLA unit is controlled by a host unit externally provided to said single chip device.

[c20] The signal chip device of claim 19, further comprising:

a first chip pin for providing a serial data path between said single chip device and said host unit; and

a second hip pin for providing a clock signal path between said single chip device and said host unit.

[c21] The single chip device of claim 17, wherein said OCLA unit comprising:

a control unit for controlling operations of said OCLA unit in response to control signals from said host unit;

a buffer capturing data processed by said signal processing unit; and

a communication unit for transferring said captured data between said VHDL macro and said host unit.